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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,397	01/05/2006	Timothy P. Gibson	H0004400	3027

128 7590 10/31/2008

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EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
10/31/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/563,397	GIBSON ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/05/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim(s) 34-42 are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus), or (2) transform underlying subject matter (such as an article or material) to a different state or thing. The instant claims neither transform underlying subject matter nor positively tie to another statutory category that accomplishes the claimed method steps, and therefore do not qualify as a statutory process.

Method claim 34, recites the steps of: receiving, generating, converting, and generating , and as explained above, a statutory "process" under 35 U.S.C. 101 must (1) be tied to another statutory category (such as a particular apparatus) and the steps of claim 34 are not tied to another statutory category that accomplishes the claimed method steps.

Dependent claims 35-42 are also rejected since they depend on claim 34 above.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent

and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-16, 45 of the instant application (10/563397) provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-9, 11-16, 18-19, 21-24, 26-28, 29 -33, 34-42, 43-45 of copending Application No. 10/616796 Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following:

The limitations of claims 1-16 of the instant application are encompassed by the limitations of claims 1- 9, 11-16 of 10/616796. The limitations of claims 18-28, 29-33, 34-42, 43-45 of the instant application are encompassed by the limitations of claims 18-19, 21-24, 26-28, 29-33, 34-342, 43-45.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

4. On page 27 of the claims, the second claim 38 is objected to because a claim 38 is already present, and the second claim 38 should be renumbered to claim 39.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 4-9, 34-37, 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Lehman et al., (U.S. 6,282,184).

With respect to claims 1, 5-9, Lehman et al., disclose: a front-end circuit operable to receive a plurality of radio signals transmitted across a frequency band (Fig. 2, front-end comprises antenna 3, and wideband receiver 40, column 2, lines 60-67, column 3, line 1, (also column 6, lines 56-66) see reception of composite RF signal containing RF signals associated with a respective standard, see also Fig. 3 (showing details of Fig. 4), frequency band is a 15MHz band, see column 6, lines 56-63 (conversion to IF), column 7, 31-47, and IF mixer 46) and generate an analog signal simultaneously

carrying a plurality of channels within said frequency band (see Fig. 3, output of BPF filter 51, a multichannel signal, see column 8, lines 11-15); an analog to digital converter coupled to said front-end circuit (Fig. 3, A/D converter 41), said analog to digital converter operable to convert said analog signal to a digital signal (column 8, lines 13-18); and a digital processing system coupled to said analog to digital converter, said digital processing system operable to receive said digital signal (Fig. 2, see digital processing system comprising blocks 7-9 (channelizers) and 13-15 DSPs) and generate at least one output signal corresponding to at least one of said plurality of channels within said frequency band (column 4, lines 6-15, separation/processing of channel of the particular protocol).

With respect to claim 4, Lehman et al., further disclose: wherein said digital processing system generates a plurality of output signals comprising a plurality of signals for transmission to a plurality of end devices (Fig. 2, see plurality of N streams generated by DSPs and they're supplied to PSTN network, (comprising a plurality of phones as end devices)).

Method claims 34-37 are rejected based on a rationale similar to the one used to reject apparatus claims 1, 6-7, and 9 respectively.

Claim 43 is rejected based on a rationale similar to the one used to reject claim 1 above.

7. Claims 1-2, 5-8, 18-19, 21-23, 28-31,33-36, 38, 41, 43-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Bexten (U.S. 6,205,133)

With respect to claim 18, Bexten discloses: at least at least one front-end circuit group comprising a plurality of front-end circuits (Fig. 7 wherein each of the receiver branches corresponds to a front-end circuit group to one and comprises a plurality of front-end circuits, 505, 215, 510, 220, column 8, lines 26-37, (some of the front-end circuit are described with respect to Fig. 2, column 3, lines 51-60)) wherein each of said front-end circuits is operable to receive a plurality of radio signals transmitted across a frequency band and generate an analog signal corresponding to a plurality of channels within said frequency band (column 8, lines 66-67, column 9, lines 5 each radio head receives an analog multi-carrier (i.e. multi-channel) signal); at least one analog to digital converter coupled to said at least one front-end circuit group (Fig. 7, see ADCs 220 coupled to each of the front end circuit groups (receiver branches), said analog to digital converter operable to receive said analog signals from said front-end circuits and convert said analog signals to a digital signal (Fig. 7, column 8, lines 26-37, 66-67,column 9 lines 1-5, where multi channel signals are captured and converted to digital form); and a digital processing system coupled to said at least one analog to digital converter (Fig. 7, blocks to the right of ADCs 220 comprise a digital processing system, since they operate on digital signals, column 8, lines 38-55), said digital processing system operable to receive said digital signal from said analog to digital converter and generate at least one output signal corresponding to at least one of said channels within

said frequency band of at least one of said front-end circuits (column 8, lines 38-55, 66-67 through column 9, lines 1-22).

With respect to claim 19, Bexten further discloses: wherein said digital processing system is operable to generate a plurality of output signals, wherein each of said output signals corresponds to at least one of said channels within said frequency band of at least one of said front end circuits (Fig. 7, outputs out of plurality of DPSs 535, supplied to switch 330, column 9, lines 5-22).

With respect to claims 21-23, Bexten further discloses: wherein each of said front-end circuits comprises an antenna circuit operable to receive said radio signals (Fig. 7 see each one of antennas 205)l wherein each one of said front-end circuits further comprises an amplifier circuit operable to amplify said received radio signals (Fig. 7, amplifiers 215); wherein at least one of said front-end circuits further comprises a filter circuit operable to filter said received radio signals (Fig. 7, BPF filters 510)

With respect to claim 28, Bexten further discloses: comprises a plurality of front end circuit groups and a plurality of corresponding analog to digital converters (Fig. 7, each one of the receiver branches) wherein said digital processing system is operable to receive a plurality of digital signals from said analog to digital converters and

generate at least one output signal corresponding to at least one of said channels within said frequency band of at least one of said front-end circuits of at least one of said front-end circuit groups (Fig. 7, blocks 315, 325, 330 comprise a digital processing system, column 8, lines 26-55, and column 9, lines 2-23).

Claims 1-2, 5-8, 43-44 are rejected based on a rationale similar to the one used to reject claims 18, 21-23 above.

With respect to claim 29, Bexten discloses: a plurality of front-end circuits each of which comprises an antenna circuit operable to receive a plurality of radio signals transmitted across a frequency band, wherein each of said front end circuits is operable to generate an analog signal corresponding to a plurality of channels within said frequency band; a plurality of analog to digital converters each of which is coupled to at least one of said front-end circuits, wherein each of said analog to digital converters is operable to receive said analog signal from said at least one of said front-end circuits and convert said analog signal to a digital signal; and a digital processing system coupled to each of said analog to digital converters, said digital processing system operable to receive said digital signals from said analog to digital converters and generate at least one output signal corresponding to at least one of said channels within said frequency band of at least one of said front-end circuits.

Claims 30, 31 are rejected based on a rationale similar to the one used to reject claims 22-23 above.

Method claims 34-36, 39 are rejected based on a rationale similar to the one used to reject claims 18, 22-23, 18 above.

8. Claims 1, 5-8, 18-23, 25, 34-36, 41, 43 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kaminski et al., (U.S. 6,678,512).

With respect to claim 1, Kaminski et al., disclose: a front-end circuit operable to receive a plurality of radio signals transmitted across a frequency band and generate an analog signal simultaneously carrying a plurality of channels within said frequency band (Fig. 3, see antenna 12a, filter 20a, amplifier 52a, frequency band 824-849MHz, see column 5, lines 40-47, see the frequency channels (simultaneously carried) within specified frequency range, received by front-end, column 5, lines 51-56); an analog to digital converter coupled to said front-end circuit (Fig. 3, A/D block 24), said analog to digital converter operable to convert said analog signal to a digital signal simultaneously carrying said plurality of channels within said frequency band (column 5, lines 62-65, column 6, lines 17-21, where the A/D receives the signals (channels) in cellular band and PCS band (see combiner shown in Fig. 3) and converts these to digital); and a digital processing system coupled to said analog to digital converter (Fig. 3, block 26, DSP), said digital processing system operable to receive said digital signal and

generate at least one output signal corresponding to at least one of said plurality of channels within said frequency band (column 4, lines 66-67 , column 5, lines 1-10, DSP retrieves digital signals (this corresponds to generating at least one output signal corresponding to at least one of said plurality of channels with said frequency band) by performing digital signal processing (and generates at least one output signal see Fig. 3 arrow out of DSP block)) .

With respect to claim 5, Kaminski et al., disclose: wherein said front-end circuit comprises an antenna circuit operable to receive said radio signals (Fig. 3, see antenna 12a).

With respect to claim 6, Kaminski et al., disclose: wherein said front-end receiver further comprises an amplifier circuit operable to amplify said received radio signals (Fig. 3, LNA, block 52a).

With respect to claims 7, 8 Kaminski et al., disclose: wherein said front-end circuit further comprises a filter circuit operable to filter said received radio signals (Fig. 3, filter 20a, bandpass filter, column 5, lines 54-56).

With respect to claims 18, 20-23, claims 18, 20-23 are rejected based on a rationale similar to the one used to reject claim 1 above, and see that Kaminski discloses: at least one front-end circuit group comprising a plurality of front-end circuits (Fig. 1, where the components to the left of the combiner block, are considered to comprise one front end circuit group see also Fig. 3).

With respect to claim 19, Kaminski further discloses: wherein said digital processing system is operable to generate a plurality of output signals, wherein each of said output signals corresponds to at least one of said channel within said frequency band of at least one of said front-end circuits (Fig. 3, where the A/D and processing block receive a plurality of signals from the combiner, in the different frequency bands Cellular and PCS, see column 6, lines 60-67 through column 7, lines 1-10, and the plurality of output signals is interpreted to correspond to the DSP outputting signals from both the PCS and cellular bands).

Method claims 34-36, 41 are rejected based on a rationale similar to the one used to reject apparatus claims 1, 6-7, 19.

Claim 43 is rejected based on a rationale similar to the one used to reject claim 1 above.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 9, 24, 32, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bexten (U.S. 6,205,133) in view of Lehman et al. (U.S. 6,282,184).

With respect to claim 9, Bexten does not expressly teach: wherein said front-end circuit further comprises an intermediate frequency mixing circuit operable to translate said received radio signals to an intermediate frequency band.

In the same field of endeavor (AMPS receivers) Lehman et al. disclose: front-end circuit further comprises an intermediate frequency mixing circuit operable to translate said received radio signals to an intermediate frequency band (column 6, lines 56-63 (conversion to IF))

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Bexten based on the teachings of Lehman et al. depending on whether the received signals had been upconverted to an intermediate frequency at the originating transmitter, and it would have been obvious to a person of ordinary skill that a corresponding downconversion to IF is required at the receiver side.

Claims 24, 32, 37 are rejected based on a rationale similar to the one used to reject claim 9 above.

11. Claims 2-4, 9-10,14-15, 17, 24-25, 27, 37, 39-40, 42, 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaminski et al., (U.S. 6,678,512) in view of Phillips et al., (U.S. 5,859,878).

With respect to claims 2-3, the limitations of these claims are not expressly disclosed by Kamiski et al., In the same field of endeavor, wireless communications, Phillips et al., disclose: wherein said digital processing system generates a single output signal comprising a time-domain multiplexed serial data link multiplexed serial data link (see Fig. 8B, (coupled to the system of 8A) where a serial interface is used to supply signals to the computer, see column 7, lines 47-52, and see Fig. 6, shows TDM processing at the receiver, that results into TDM outputs); further comprising a controller coupled to said digital processing system, said controller operable to receive said time-domain multiplexed serial data link and generate a plurality of signals to a plurality of end devices (Fig. 12B, line transceiver and system bus, supplying serial data to plurality of end devices in computer, column 16, lines 14-17, uart (serial communication), and see column 15, lines 50-56).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminski et al., based on the teachings of Phillips et al., to achieve high-speed transfer of data (TDM serial data) and supply data to a plurality of external users (intercom).

With respect to claim 4, Kaminski further discloses: wherein the digital processing system generates a plurality of output signals (Fig. 3 DSP has PCS and Cellular band output signals).

In the same field of endeavor, wireless communications, Phillips et al., disclose: generate a plurality of signals comprising a plurality of signals for transmission to a plurality of end devices (Fig. 12B, line transceiver and system bus, supplying serial data to plurality of end devices in computer, column 16, lines 14-17, uart (serial communication), and see column 15, lines 50-56).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminski et al., based on the teachings of Phillips et al., to supply data to a plurality of external users (intercom).

With respect to claim 9, Kaminski does not expressly teach: wherein said front-end circuit further comprises an intermediate frequency circuit operable to translate said received radio signals to an intermediate frequency band.

In the same field of endeavor, Phillips discloses: a front-end circuit further comprises an intermediate frequency circuit operable to translate said received radio signals to an intermediate frequency band (column 6, lines 5-10, downconversion to IF frequency).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminski based on the teachings of Phillips depending on whether the received signals had been upconverted to an intermediate

frequency at the originating transmitter, and it would have been obvious to a person of ordinary skill that a corresponding downconversion to IF is required at the receiver side.

With respect to claim 10, Kaminski further discloses: a digital downconverter operable to select said at least one of said channels within said frequency band; and a digital processor operable to generate said at least one output signal (Fig. 3, function of block 26 DSP processor and see the generated output signal(s), column 4, lines 66-67, column 5, lines 1-9);

Kaminski does not expressly teach: the digital processor operable to extract information from said at least one of said channels and generate said at least one output signal.

In the same field of endeavor, wireless communications, Phillips discloses: a digital processor operable to extract information from said at least one of a plurality of channels and generate said at least one output signal (Fig. 3A DSP 216, column 10, lines 49-65 column 23, lines 5-7, 24-28).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminksi et al. based on the teachings of Phillips so that information is extracted from the selected channel, since the purpose of a receiver is to extract information that was transmitted.

With respect to claim 14, Kaminski does not expressly teach: wherein said digital signal processor extracts information from said at least one of said selected channels according to configurable channel decoding parameters.

In the same field of endeavor, Phillips discloses: wherein said digital signal processor extracts information from said at least one of said selected channels according to configurable channel decoding parameters (column 10, lines 49-58).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminksi based on the teachings of Phillips to process (decode) a variety of received signals using flexible-programmable processing functions (Phillips, column 10, lines 49-54)

With respect to claim 15, Kaminski does not expressly teach: wherein said configurable channel decoding parameters are software configurable.

In the same field of endeavor, Phillips discloses: wherein said configurable channel decoding parameters are software configurable (column 22, lines 61-67 column 23 lines 1-3 and column 11, lines 49-51, DPS executes a RAM program to perform signal processing/decoding).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminksi based on the teachings of Phillips to process (decode) a variety of received signals using flexible-programmable processing functions (Phillips, column 10, lines 49-54, column 11, lines 25-32).

With respect to claim 17, Kaminski does not expressly teach: wherein said digital signal processor controls said digital down converter.

In the same field of endeavor, Phillips discloses: wherein said digital signal processor controls said digital down converter (column 11, lines 39-54, 62-66 where the DDC is the digital downconverter, column 10, lines 40-48).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminksi based on the teachings of Phillips to achieve fast system reconfiguration using programmed application programs (Phillips, column 10, lines 49-54, column 11, lines 25-32, 39-41, 63-65).

Claims 24-25, 27 are rejected based on a rationale similar to the one used to reject claims 9-10, 15 above,

With respect to claims 37, 39 (numbered as a second claim 38 in the claims received on 1/05/06 but should be numbered as claim 39) 40, 44-45 see above rejection of claims 9, 2,4 (time-domain multiplexed signals correspond to a plurality of output signals).

9. Claims 11-13, 16, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaminski et al., (U.S. 6,678,512) in view of Phillips et al., (U.S. 5,859,878) and further in view of Bugeja et al. (U.S. 2002/0177446).

With respect to claim 11, neither Kaminski nor Phillips et al. expressly teach: wherein said digital down converter selects said at least one of said channels according to configurable channel selection parameters.

In the same field of endeavor, Bugeja et al. discloses: a digital down converter selecting at least one of said channels according to configurable channel selection parameters (Fig. 1, blocks controller 30, Digital baseband and Mac Layer 22, ¶0032-0034, and Fig. 6 ¶0059-0060 see programmable center frequencies and bandwidths of programmable filters and programmable digital downconverters, 124a-124N, 126a-126N)

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminski and Phillips so that a bandwidth and frequency of a channel are programmable, resulting in a flexible (programmable) receiver system.

With respect to claims 12,13 Bugeja et al. further discloses: wherein said configurable channel selection parameters are software configurable; wherein said configurable channel selection parameters are selected from the following group: channel frequency, channel bandwidth, and combinations thereof. (Fig. 1, blocks controller 30, Digital baseband and Mac Layer 22, ¶0032-0034, and Fig. 6 ¶0059-0060 see programmable center frequencies and bandwidths of programmable filters and programmable digital downconverters, 124a-124N, 126a-126N)

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminski and Phillips based on the teachings of Bugeja et al. so that a bandwidth and frequency of a channel are programmable, resulting in a flexible (programmable) receiver system.

With respect to claim 16, Kaminski and Phillips further disclose: wherein said configurable channel decoding parameters are selected from the following group: channel frequency, channel modulation scheme, channel information format, and combinations thereof (Phillips column 10, lines 49-58).

Neither Kaminski nor Phillips expressly teach: channel bandwidth.

In the same field of endeavor, Bugeja et al. further discloses: configurable channel decoding parameters are selected from: channel bandwidth (Fig. 1, blocks controller 30, Digital baseband and Mac Layer 22, ¶0032-0034, and Fig. 6 ¶0059-0060 see programmable bandwidths of programmable filters).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Kaminski and Phillips based on the teachings of Bugeja et al. so that channel bandwidth is programmable, resulting in a flexible (programmable) receiver system.

Claim 26 is rejected based on a rationale similar to the one used to reject claim 11 above.

Claim 38 is rejected based on a rationale similar to the one used to reject claims 11 and 16 above.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is (571)272-5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SOPHIA VLAHOS/
Examiner, Art Unit 2611
10/24/2008

/Mohammad H Ghayour/
Supervisory Patent Examiner, Art Unit 2611